NANO-METRIC OPTIMISED CMOS RF RECEIVER FRONT-END COMPONENTS FOR UHF RFID READERS

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ABSTRACT

Nano-metric Optimised CMOS RF Receiver Front-end Components for UHF RFID Readers

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As the capabilities of wireless hand-held devices continue to increase, more pressure is placed on the performance of RF transceiver front-ends. The primary objective of this research is to investigate optimal methods of implementing a receiver front-end with reduced power dissipation, reduced design complexity and minimised cost. This design will be implemented on CMOS technology due to its advantages in system integration and low-cost mass production.

This thesis presents the optimisation of a CMOS RF receiver front-end components design for 866 MHz UHF RFID readers. The completed receiver front-end was fabricated on an IBM 130nm CMOS process. Circuit-level techniques were employed to reduce chip size and power consumption while providing enhanced performance. The inclusion of the finite drain-source conductance g_{ds} effect improves the nano-metric design optimisation algorithm. Simulated results and experimental data are presented that demonstrate the RF receiver design with low power dissipation and low noise while providing high performance.

Low-noise amplifiers using a power-constrained simultaneous noise and input matching (PCSNIM) technique are presented first. In contrast to previously published narrow-band LNA designs, the proposed design methodology includes the finite drain-source conductance of devices, thus achieving simultaneous impedance and minimum noise matching at the very low power drain of 1.6mW from a 1V supply. The LNA delivers a power gain (S21) of 17dB, a reverse isolation (S12) of -34dB and an input power

reflection (S11@866 MHz) of -30dB. It has a minimum pass-band NF of around 2dB and a 3rd order input referred intercept point (IIP3) of -16dBm.

A low noise mixer is also presented utilising the PCSNIM topology with current bleeding techniques. This design is proposed to replace the conventional Gilbert cell mixer that usually exhibits a high noise figure. The proposed mixer has demonstrated the ability to scale to the targeted 130nm process and meets design requirement at the required operating frequency. It has a power conversion gain of 14.5dB, DSB noise figure of 8.7dB DSB and an IIP3 of -5.1dBM. The mixer core itself only consumes 6mW from a 1.2V supply and the complete test circuit consumes 10mW with a balun at each port.

Finally, a voltage controlled oscillator (VCO) is presented. A quadrature VCO (QVCO) structure is selected to overcome the image rejection issue. Since the main goal for this work is to design a low power receiver front-end, a folded-cascode topology is employed to enable the QVCO to operate under 1V power supply. The proposed VCO has a phase noise of -140dBc/Hz at 3-MHz offset from the carrier with only 5mW of power dissipation. This gives a FoM value of -181dBc/Hz that compares favourably to recently published designs.

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Dedicated to my parents

DECLARATION

The author declares that this is his own work except where due acknowledgement has been given. It is being submitted for the PhD in Engineering to Massey University, New Zealand.

This thesis describes the research carried out by the author at the School of Engineering, Massey University, New Zealand from February 2007 to February 2011, supervised by Dr. Rezaul Hasan.

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

DEFINITIONS AND ABBREVIATIONS

3G	Third Generation
AC	Alternating Current
ADS	Agilent's Advanced Design System program
AM	Amplitude Modulation
BB	Baseband
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CG	Common-gate
CP	Compression Point
DAC	Digital to Analog Converter
DC	Direct Current
DRC	Design Rule Check
DSP	Digital Signal Processing
DUT	Device / Die Under Test
EDGE	Enhanced Data rates for GSM Evolution
ESD	Electrostatic Discharge
F	Noise factor
FFT	Fast Fourier Transform
FM	Frequency Modulation
FSK	Frequency Shift Keying
GaAs	Gallium Arsenide
GDSII	Gerber Data Stream Information Interchange
GHz	Gigahertz
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
Hz	Hertz

HF	High Frequency
I/O	Input-Output
IC	Integrated Circuit
IEEE	The Institute of Electrical and Electronics Engineers, Inc.
IF	Intermediate Frequency
IIP3	Input Third Order Intercept Point
IM	Inter-modulation
IM3	Third Order Inter-modulation
IP2	Second Order Intercept Point
IP3	Third Order Intercept Point
ISF	Impulse Sensitivity Function
I/Q	In phase-Quadrature phase
KCL	Kirchoff Current Law
KVL	Kirchoff Voltage Law
LAN	Local Area Network
LC	Inductor-Capacitor
LF	Low Frequency
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Lower Sideband
LTI	Linear Time-Invariant
LTV	Linear Time Varying
LVS	Layout versus Schematic
MIMO	Multiple Input – Multiple Output
MCM	Multi Carrier Modulation
MOS	Metal Oxide Semiconductor
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
P1dB	1-dB Gain Compression Measurement
PA	Power Amplifier
PGS	Patterned Ground Shield
PSK	Phase Shift Keying
PSRR	Power Supply Rejection Ratio

PSS	Periodic Steady State
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
Rx	Receiver
SAW	Surface Acoustic Wave
SCM	Single Carrier Modulation
SNR	Signal to Noise Ratio
SoC	System on Chip
SSB	Single Sideband
Tx	Transmitter
UHF	Ultra-high Frequency
UMTS	Universal Mobile Telecommunications System
USB	Upper Sideband
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VNA	Vector Network Analyser
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Networks
XDB	Gain Compression